This Listing of Claims will replace all prior versions or listings of claims in this application.

LISTING OF CLAIMS:

1. (Currently Amended) An integrated circuit to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the integrated circuit comprising:

a plurality of memory blocks, each of the memory blocks comprising a plurality of sub-memory blocks;

a plurality of data memory blocks corresponding to the memory blocks, wherein each of the data memory blocks has the same size as a sub-memory block; and

a tag memory controlling unit, which writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address, wherein ~~a write operation or a read operation is performed in a data memory block and one of the write operation and the read operation not performed in the data memory block is performed in a sub-memory block when access to the sub-memory block and corresponding data memory block is simultaneously performed when the write address and the read address are the same~~ when the write address and the read address are the same as the data memory address, the read operation is performed in the data memory block and the write operation is performed in the sub-memory block, and wherein when the write address and the read address are both not the same as the data memory address, the operation corresponding to the address that is the same as the data memory address is performed in the data memory block and the operation corresponding to the address that is not the same as the data memory address is performed in the sub-memory block.

2. (Original) The integrated circuit of claim 1, wherein the sub-memory blocks are a set of memory cells for sharing a common word line or bit line.

3. (Original) The integrated circuit of claim 1, wherein in the sub-memory blocks, two or more word lines or bit lines cannot be simultaneously activated.

4. (Canceled)

5. (Previously Presented) The integrated circuit of claim 1, wherein the data memory blocks have a number of columns and rows different from a number of columns and rows of the sub-memory block.

6. (Original) The integrated circuit of claim 1, wherein the tag memory controlling unit has a same number of decoding addresses as a number of addresses for decoding the data memory blocks.

7. (Original) The integrated circuit of claim 6, wherein the tag memory controlling unit has a number of columns and rows different from a number of columns and rows of the data memory blocks.

8. (Original) The integrated circuit of claim 1, wherein the tag memory controlling unit stores a data memory address indicating that data stored in the data memory blocks is originally data corresponding to one of the sub-memory blocks, and validity determination information for determining whether data stored in the data memory block is valid.

9. (Original) The integrated circuit of claim 8, wherein if the number of the sub-memory blocks is 2N, each address of the tag memory controlling unit includes N+1 data bits,

and N-bit of the N+1 data bits indicates a data memory address, and remaining 1-bit of the N+1 data bits indicates the validity determination information.

10. (Original) The integrated circuit of claim 1, wherein the data memory blocks have a direct mapping relation with the sub-memory blocks.

11. (Original) The integrated circuit of claim 1, wherein the data is input or output at a single data rate (SDR) or a double data rate (DDR).

12. (Currently Amended) A method for simultaneously performing a write operation and a read operation in an integrated circuit ~~comprising~~ having a separate input and output and a plurality of data memory blocks and a plurality of sub-memory blocks, the method comprising:

determining if a write address and a read address have been input during a period of a clock signal;

determining if an upper address of the write address is the same as an upper address of the read address, when the write address and the read address have been input during the period of the clock signal; and

performing a write operation ~~or~~ and a read operation ~~in a data memory block and performing one of the write operation and the read operation not performed in the data memory block in a sub-memory block during one period of the clock signal when the upper addresses of the write and read addresses are the same~~ such that upon determining that the write address and the read address are the same as a data memory address, the read operation is performed in the data memory block and the write operation is performed in the sub-memory block and upon determining that the write address and the read address are both not the same as the data memory address the operation corresponding to the address that is the same as the data memory address is

performed in the data memory block and the operation corresponding to the address that is not the same as the data memory address is performed in the sub-memory block.

13. (Canceled)

14. (Canceled)

15. (Previously Presented) The method of claim 12, further comprising:

determining if the write address and the read address are the same as a data memory address, when it is determined that the upper address of the write address and the upper address of the read address are the same;

determining if only one of the write address and the read address is coincident with the data memory address or if both the write address and the read address are coincident with the data memory address, when both the write address and the read address are the same as the data memory address; and

performing the read operation in the data memory block and the write operation in the sub-memory block during one period of the clock signal, when both the write address and the read address are not coincident with the data memory address; or

performing an operation corresponding to the address coincident with the data memory address in the data memory block and an operation corresponding to the address not coincident with the data memory address in the sub-memory block during one period of the clock signal, when only one of the read address and the write address is coincident with the data memory address.

16-20. (Canceled)

21. (Previously Presented) An integrated circuit to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the integrated circuit comprising:

a plurality of memory blocks, each of the memory blocks comprising a plurality of sub-memory blocks;

a plurality of data memory blocks corresponding to the memory blocks; and

a tag memory controlling unit, which writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address, wherein access to the same sub-memory block is not simultaneously performed when the write address and the read address are the same,

wherein the tag memory controlling unit has a same number of decoding addresses as a number of addresses for decoding the data memory blocks and a number of columns and rows different from a number of columns and rows of the data memory blocks.

22. (Canceled)